# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 5206 | 438/22,24,48,106,110,115.ccls. | US-PGPUB; USPAT | OR | OFF | 2006/03/09 09:25 |
| L2 | 3988 | 1 and @ad<"20031007" | US-PGPUB; USPAT | OR | OFF | 2006/03/09 09:25 |
| L3 | 2371 | 2 and (etch or etching) | US-PGPUB; USPAT | OR | OFF | 2006/03/09 09:26 |
| L4 | 3 | ((etch or etching) and (insulative or insulating or insulator or dielectric) and (micro with solution) and diameter).clm. | US-PGPUB; USPAT | OR | OFF | 2006/03/09 09:28 |

US-PAT-NO: 5108553

DOCUMENT-IDENTIFIER: US 5108553 A

TITLE: G-tab manufacturing process and the product produced thereby

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Claims Text - CLTX (8):
4. The method of claim 3 wherein said aperture is patterned to have a **diameter** of from about 2 mils to about 10 mils.

Claims Text - CLTX (9):
5. The method of claim 4 wherein said aperture is patterned to have a **diameter** of from about 3 mils to about 5 mils.

Claims Text - CLTX (10):
6. The method of claim 4 wherein said non-conductive via is formed by ablating said **dielectric** layer with a laser.

Claims Text - CLTX (14):
(1)carbon black particles having an average particle **diameter** of less than about 3.0 microns in said dispersion;

Claims Text - CLTX (29):
(b) connecting said first and second conductive planes with at least one non-conductive hole via having a **diameter** of up to about 5 mils;

Claims Text - CLTX (34):
20. The method of claim 19 wherein said through hole has a **diameter** of from about 1 mil to about 2 mil.

Claims Text - CLTX (35):
21. The method of claim 19 wherein said non-conductive through hole via is formed by ablating said **dielectric** layer with a laser.

Claims Text - CLTX (39):
(1) carbon black particles having an average particle **diameter** of less than about 3.0 microns in said dispersion;

Claims Text - CLTX (60):
36. The method of claim 35 wherein said dispersion of carbon black is removed from said first and second conductive planes by micro **etching**.

Claims Text - CLTX (61):
37. The method of claim 36 wherein a sodium persulfate **solution** is utilized for **micro etching**.

Claims Text - CLTX (67):
40. The method of claim 32 wherein said aperture forms a template to locate and limit the **diameter** of said non-conductive via.

Claims Text - CLTX (72):
45. The method of claim 44 wherein said aperture is patterned to have a **diameter** of from about 2 mils to about 10 mils.

Claims Text - CLTX (73):
46. The method of claim 45 wherein said aperture is patterned to have a **diameter** of from about 3 to about 5 mils.

Claims Text - CLTX (75):
48. The method of claim 47 wherein said through hole has a **diameter** of up to about 5 mils.

Claims Text - CLTX (76):
49. The method of claim 48 wherein said through hole has a **diameter** of from about 1 to about 2 mils.

DOCUMENT-IDENTIFIER: US 20040201107 A1

TITLE: Transistor assembly and method for the production thereof

---------- KWIC ---------

Claims Text - CLTX (9):
8. A method of fabricating a transistor arrangement, characterized by the fact that a metal layer is embedded between two plastic films, that ion trace channels are introduced into this laminate film by ion bombardment, that the film laminate is subsequently subjected to an **etching** treatment, that the ion trace channels etched to micro holes are filled with semiconductor material and that by metal coating source or drain contacts are formed on the upper and lower surface of the film laminate.

Claims Text - CLTX (10):
9. The method of claim 8, characterized by the fact that the metal layer between the plastic films is subjected within the micro holes to a special **etching** treatment.

Claims Text - CLTX (11):
10. The method of claim 9, characterized by the fact that for forming field effect transistors the micro holes are provided with an **insulating** layer.

Claims Text - CLTX (12):
11. The method of claim 8 or 9, characterized by the fact that for forming field effect transistors the metal layer in the area of the micro holes is etched away to behind the **diameter** of the micro holes.

Claims Text - CLTX (16):
15. The method of one of claims 8 to 14, characterized by the fact that the **etching** treatment of the ion trace channels results in the formation of micro holes of a **diameter** between 30 nm and 20 .mu.m.

Claims Text - CLTX (19):
18. The method of one of claims 8 to 17, characterized by the fact that the **etching** of the ion trace channels is carried out with a sodium hydroxide solution.

Claims Text - CLTX (22):
21. The method of one of claims 8 to 20, characterized by the fact that that prior to **etching** of the ion trace channels the film laminate is treated with a sensitizing agent.

Claims Text - CLTX (26):
25. The transistor assembly of claim 24, wherein micro holes are of a **diameter** between 30 nm and 20 .mu.m.

Claims Text - CLTX (33):
32. A method of fabricating a transistor assembly, comprising the steps of: providing a film laminate comprising first and second layers of pliable film with a metal layer therebetween; subjecting the film laminate to ion bombardment to provide a plurality of ion trace channels therein; **etching** the film laminate to an **etching** process to convert the ion trace channels to micro holes; vertically introducing into the micro holes a semiconductor material; and metal coating at least one of the outer surfaces of the film laminate to provide at least one electrical contact connected to the semiconductor material.

Claims Text - CLTX (34):
33. The method of claim 32, further comprising the step of subjecting the metal layer between the layers of pliable film to an **etching** process within the micro holes.

Claims Text - CLTX (35):
34. The method of claim 33, further comprising the step of lining the micro holes with an **insulating** layer to form a field effect transistor.

Claims Text - CLTX (36):
35. The method of claim 34, further comprising the step of **etching** away the metal layer in the area of the micro holes beyond the **diameter** of the micro holes to form a field effect transistor.

Claims Text - CLTX (42):
41. The method of claim 32, wherein the step of **etching** for converting the ion trace channels to **micro** holes is carried out in a **solution** of sodium hydroxide.

Claims Text - CLTX (45):
44. The method of claim 40, further comprising the step of subjecting the film laminate to a sensitizing agent prior to **etching**.